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To: Examiner Long Pham

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Applicants	: Jigish D. Trivedi
Serial No.	: 08/915,658
Filed	: August 21, 1997
Title	: LOW RESISTANCE METAL SILICIDE LOCAL INTERCONNECTS AND METHOD OF MAKING
Docket No.	: MIO 0024 PA
Examiner	: Long Pham
Art Unit	: 2814

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PAGE 1/4 * RCVD AT 10/23/2006 2:13:15 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-5/2 * DNIS:2738300 * CSID:9374496405 * DURATION (mm-ss):01-02

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

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Susan M. Luna
Agent Reg. No. 38,769

Sir:

RESPONSE TO NOTIFICATION OF NON-COMPLIANT APPEAL BRIEF

(37 CFR §41.37)

This paper is being filed in response to the Notification of Non-Compliant Appeal Brief (37 CFR §41.37) mailed October 12, 2006. Pursuant to MPEP §1205.03,

> (B) When the Office holds the brief to be defective solely due to appellant's failure to provide a summary of the claimed subject matter as required by 37 CFR 41.37(c)(1)(v), an entire new brief need not, and should not, be filed. Rather, a paper providing a summary of the claimed subject matter as required by 37 CFR 41.37(c)(1)(v) will suffice.

Accordingly, appellants are providing herewith a revised Summary of the Claimed Subject Matter in compliance with the rule.

Summary of Claimed Subject Matter

The present invention is directed to a low resistance local interconnect which is formed by providing a metal layer over a semiconductor layer, forming a metal silicide layer over the layer of metal, annealing the layers to form a composite structure, and removing unreacted metal from the metal layer.

Concise explanation of the Subject Matter Defined in Independent Claim 31 and dependent claims 32-34

Referring to Figs. 3-7 and the specification at page 12, lines 12-29 and page 13, lines 1-16, a composite structure is shown which is formed from a layer of a first metal silicide 34 which is formed over a metal layer 32 (Fig. 3). A layer of photoresist 36 is formed over the metal silicide layer 34 (Fig. 4) and is patterned and etched to form a structure 34A (Fig. 5) which defines the boundaries of the local interconnect. The patterned structure 34A is then reacted with the underlying metal layer 32 by annealing to form a composite structure 37 (Fig. 6). The resulting composite structure 37 includes the first metal silicide, a second metal silicide (formed by the reaction of silicon from first metal silicide 34 with underlying metal 32), and an intermetallic compound which comprises metal from the first metal silicide 34 and metal from the underlying metal layer 32.

As described in the specification at page 7, lines 8-12, the first and second metal silicides each comprise at least one refractory metal selected from chromium, cobalt, molybdenum, nickel, niobium, palladium, platinum, tantalum, titanium, tungsten, and vanadium. The first metal silicide may comprise titanium silicide and the second metal silicide may comprise tungsten silicide.

Concise explanation of the Subject Matter Defined in Independent Claim 41 and dependent claims 43 and 48-49

As described in the specification at page 13, lines 6-17, the intermetallic compound in the composite structure is formed by a reaction between the first metal silicide and the second metal silicide. The titanium tungsten intermetallic compound reduces the resistance of the local interconnect.

Concise explanation of the Subject Matter Defined in Independent Claim 35 and dependent claims 36 and 42

As described in the specification at page 11, lines 20-28, the local interconnect comprising the composite structure may be used to connect a first active semiconductor region to a second active semiconductor region on a substrate assembly. For example, as shown in Figs.

3-7, the local interconnect may be used to connect a gate (G) of one MOSFET to the drain (D) or source (S) of another MOSFET. As shown, the first and second active semiconductor regions are separated by an insulating region (field oxide 16). As described at page 7, line 22, the composite structure has a thickness of about 700 Angstroms to about 1800 Angstroms.

Concise explanation of the Subject Matter Defined in Independent Claim 37 and dependent claims 44-45

As shown in Fig. 8 and as described in the specification at page 14, lines 20-22, one or more interconnects 37 may also be used to connect various structures in an integrated circuit 40, such as the gates of two or more transistors 14, and respective sources to respective drains.

Concise explanation of the Subject Matter Defined in Independent Claim 38 and dependent claims 39-40 and 46-47

As shown in Figs. 9 and 10 and as described in the specification at page 14, lines 22-29 and page 15, lines 1-9, one or more local interconnects 37 comprising the composite structure may be used in a memory array such as a static random access memory (SRAM) or a dynamic random access memory (DRAM). The memory array includes a plurality of memory cells 46 arranged in rows and columns and formed on a substrate having at least one semiconductor layer, with each of the plurality of memory cells comprising at least one field effect transistor 14. The local interconnect connects at least one of a source, drain or gate of the field effect transistor in one of the plurality of memory cells to an active area within one memory cell or to one of a source, drain, or gate of the field effect transistor in another one of the plurality of memory cells.

Respectfully submitted,
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